Pattern Recognition, p. 767, Virtual Event, 2021]. DOI: doi.org/ 10.48550/arXiv.2011.12276.

8. Mazzone M., Elgammal A. (2019). Art, Creativity, and the Potential of Artificial Intelligence, *J. Arts,* vol. 8(1), 2-9. DOI: https://doi.org/ 10.3390/arts8010026

9. Pylypchuk O. Certificate of depositing the result of intellectual activity № 190–РІД/Ук–2020. Algorithm for the computer program "CONCORDIA" harmonization of the colour of the interior environment and works of fine art. State Scientific and Technical Library of Ukraine. Kyiv, 12.10.2020.

10. Pylypchuk O., Polubok A., Krivenko O., Safronova O., Kosenko D., Avdieieva N. (2021). Developing an Approach to Colour Assessment of Works of Art with Aim to Creating a Comfortable and Harmonious Interior. Proceedings of the International Conference on Social Sciences and Big Data Application, Dec. 10–12, Xi'an, China. *J. of Advances in Social Science, Education and Humanities Research, Atlantis Press SARL, Part of Springer Nature*, Vol. 614, 181–187. DOI: https://doi.org/10.2991/ assehr.k.211216.036.

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A MODEL FOR CREATING FAILURE-RESISTANT INFORMATION-MANAGEMENT SYSTEMS FUNCTIONING IN THE SYSTEM OF RESIDUAL CLASSES

МОДЕЛЬ СТВОРЕННЯ ВІДМОВОСТІЙКИХ ІНФОРМАЦІЙНО-КЕРУЮЧИХ СИСТЕМ, ФУНКЦІОНУЮЧИХ У СИСТЕМІ ЗАЛИШКОВИХ КЛАСІВ

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The increased requirements for ensuring reliability, fault tolerance and performance for modern information and control systems (ICS) necessitate a constant search, development and implementation of advanced technologies and methods of information processing focused on a specific area of application. However, despite the intensive development of modern information technologies (IT) used in the creation of hardware and software for ICS, there are many unsolved task and problems in this area.

An analysis of promising directions for the development of information and control systems showed that new opportunities in the field of improving and further developing ICS are directly related to the transition to the implementation of parallel computing, provided that such systems are highly fault-tolerant [1, p. 494].

In principle, parallelization can be carried out at several levels: at the level of creation and implementation of physical models of objects and processes; at the level of creating mathematical models that allow organizing parallel processing of information; at the level of the solution method; at the level of algorithms of known methods; at the program level; at the level of arithmetic operations; at the level of information exchange in the ICS; data input and output, etc. A promising direction in the development of high-performance and fault-tolerant ICS is the transition to parallelization at the level of arithmetic micro-operations [2, p. 256].

The reserve for increasing the performance of the ICS is the use of systems whose architecture is adequate to the algorithm of the problem and applying the principles of parallelization at different levels [3, p. 16].

The search and study of ways to improve the fault tolerance of real-time ICS without reducing the performance of information processing showed that, on the one hand, within the positional number system (PNS), this is practically impossible to achieve without a significant deterioration in the weight, size and other basic characteristics of the ICS. On the other hand, studies carried out in the direction of developing the theory and practice of non-positional coding and using it to build super-efficient and highly reliable ICS, both by domestic and foreign scientists (Valakh M., Svoboda A., Sabo

N., Aksushskyi I.Y., Yuditskyi D.I., Glushkov V.M., Torgashov V.A., Amberbaev V.M., Kolyada A.A., Shimbo A., Paulier P., Thornton M.A., Dreschler R., Miller D.M., and others) showed that the use of a non-positional system of residual classes (SRC) as a number system for an ICS can positively solve the scientific and applied problem of ensuring the fault tolerance of an ICS without reducing the user's information processing performance with a significantly smaller amount of additionally introduced equipment than in the PNS.

In this regard, it is advisable to note the relationship and influence on the process of functioning of information processing systems of the following main properties of the SRC [4, p. 8].

The property of low-bit residuals of the SRC can significantly increase the reliability and speed of performing modular operations, both due to the low-bit information processing paths (IPP), and due to the possibility of effective use, in contrast to the SRC, tabular arithmetic. In this case, addition, subtraction and multiplication operations are performed in almost one clock cycle, which significantly increases the performance of modular operations.

This property allows the use of many different principles for the implementation of modular operations, which significantly expands the list of options for system engineering solutions used in the creation of ICS.

The property of independence of the residuals of the SRC allows you to create an ICS in the form of a set of independent, parallel operating IPPs (separate "small" IPPs that operate according to their specific modulus m_i in the SRC, independently of each other). Thus, the ICS functioning in the SRC has a modular design, which allows maintenance and troubleshooting without stopping the information processing process, while repair and preventive maintenance does not require highly qualified personnel. The time of implementation of modular operations in the ICS is determined by the time of implementation of the operation in the IPP according to the largest base m_i SRC.

Errors that occur due to failures (failures) of binary digit circuits in an arbitrary IPP do not "multiply" into neighboring paths (remain within one residue), which makes it possible to increase the reliability of information processing in the SRC. In this case, it does not matter whether there was a single or multiple error or a burst of errors no longer than $[log_2(m_i - 1)]+1$ bits. An error that occurred in the IPP based on m_i is either stored in this path until the end of the calculations, or is eliminated in the process of further calculations (for example, if after a failure occurs in the remainder a_i, the intermediate result is multiplied by a number that has a zero digit in base m_i).

Thus, this SRC property makes it possible to implement a unique system for monitoring and correcting errors in the dynamics of the information processing process with the introduction of a minimum code redundancy without stopping calculations, which is essential for systems operating in real time, for example, by introducing an alternative set of numbers. A detailed study of this property made it possible to conclude that devices operating in the SRC can be attributed to easily controlled and easily diagnosed objects, and this suggests the possibility of developing effective methods for monitoring, diagnosing and correcting information errors in the ICS.

The property of equality of residuals is as follows. Any remainder a_i of the number $A = (a_1, a_2, \ldots, a_n)$ carries information about the entire original number, which makes it possible to programmatically replace the failed IPP, modulo mi, with a workable path modulo m_j ($m_i < m_j$) without interrupting the solution of the problem. Thus, the ICS functioning in the SRC, having, for example, two control bases, retains its operability in case of failure of any two of the IPP. If failures occur in the third or fourth paths, the ICS continues to execute the information processing program, with some decrease in the accuracy of calculations, i.e. The ICS has the property of gradual degradation while maintaining the main technical characteristics. This property determines the characteristic feature of the functioning of the ICS in the SRC – the same information processing device (IPD), depending on the requirements, may have different reliability, calculation accuracy and speed in the dynamics of the information processing process, i.e. in the process of solving the problem, one can vary the reliability, accuracy of calculations, and speed.

The analysis of the properties of the SRC considered above allows us to speak about the possibility of implementing three main types of redundancy in the ICS simultaneously: structural, informational and functional, such an implementation seems possible when the second and third properties are used together.

In PNS (unlike SRC), the use of one type of reservation does not always lead to the simultaneous presence of other types of reservation. Note that this does not indicate the absence of other types of redundancy. Thus, the use of information redundancy (introduction of information redundancy) to improve the reliability of information processing causes the presence of structural secondary redundancy. Thus, the use of the required type of redundancy in the PNS is necessarily accompanied by the presence of unused ("harmful") structural redundancy, which, ultimately, negatively affects the technical and cost characteristics of the ICS [5, p. 3].

A study of developments in the scientific field under consideration has shown that there is an objective contradiction between the simultaneously high requirements for ensuring the fault tolerance of the functioning of real-time ICS and the performance of information processing in such a system. This contradiction is due to the following circumstances:

– limited capabilities of the existing ICS operating in the positional number system to carry out in real time both highly reliable and high-speed parallel implementation of computing processes;

– increased requirements for the simultaneous provision of both the performance of information processing in real time and the reliability of the functioning of the ICS.

To eliminate this contradiction, this material formulates a model for creating fault-tolerant real-time information and control systems that operate in a system of residual classes without reducing the performance of information processing.

References:

1. Avizienis, A. A fault tolerance infrastructure for dependable computing with high-performance COTS components. *Annual IEEE/IFIP Internetional Conference on Dependable Systems and Networks (DSN-2000):* materials of the 30-th internetional conference. (New York, June 2000). New York, 2000. P. 492–500.

2. Барсов В. И. Методология параллельной обработки информации в модулярной системе счисления : монография / В. И. Барсов, Л. С. Сорока, В. А. Краснобаев. Харьков : МОНУ, УИПА, 2009. 268 с.

3. Мельник А. О. Архітектура комп'ютера / А. О. Мельник. Луцьк : Волинська обласна друкарня, 2008. 470 с.

4. Акушский И. Я., Юдицкий Д. М. Машинная арифметика в остаточных классах. Москва: Советское радио, 1968. 440 с.

5. Noura H., Theilliol D., Ponsart J.-C., Chamseddine A. Fault-tolerant Control Systems. *Design and Practical Applications. Series: Advances in Industrial Control*. United Kingdom, 2009. 233 p.